e-Quals Unit Syllabus

Level 3 Digital Electronics 3 (7267-526)

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Unit 526 Digital Electronics 3

Rationale

This unit concerns the characteristics of logic families and their use in sequential logic circuits and faultfinding on prepared circuit boards.

Learning outcomes

There are **four** performance outcomes for this unit. The candidate will be able to demonstrate an:

- understanding of logic families and the terms used in their specifications
- understanding time division multiplex (TDM)
- understanding of sequential logic
- appreciation of common fault types and an understanding of fault-finding procedures and test equipment.

Assessment and grading

Assessment will be by means of a **set assignment** covering both practical activities and underpinning knowledge..

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Outcome 1 Demonstrate an understanding of logic families and the terms used in their specifications

Practical activities

The candidate will be able to:

1 use a slowly changing voltage applied to a device in a number of different families to determine the threshold levels

2 investigate the result of leaving inputs floating by deducing the value from the gate output voltage

3 connect a gate to a variety of loads and drive a gate from a variety of input sources.

Underpinning knowledge

The candidate will be able to:

1 identify the main characteristics of digital logic devices that aid selection

- i. device numbering
- ii. packaging SIL, DIL, surface mount
- iii. pin numbering
- iv. open collector

2 describe the meaning and significance of the following terms

- i. circuit features for switched ranges.
- ii. block diagrams
- iii. frequency limitations
- iv. low level input voltage
- v. noise margin
- vi. input current (logic high and low)
- vii. output current
- viii. rise and fall time
- ix. propagation delay
- x. power dissipation
- xi. absolute maximum ratings
- xii. fan-out

3 identify the main characteristics of the logic families, to include benefits and limitations of the

- i. 4000 series

ii. 74LS series

iii. 74HC series

iv. 74HCT series

v. 74AHC series

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Outcome 2 Demonstrate an understanding of time division multiplex (TDM)

Practical activities

The candidate will be able to:

1 connect two digital circuits via a fibre optic link

2 use time division multiplexing to transmit a number of separate transmissions through a single transmission path

3 use logic tutors to investigate the operation and confirm data sheet information for each circuit.

Underpinning knowledge

The candidate will be able to:

1 identify the requirements of a communication link using time division multiplexing (TDM)

- i. sampling and choice of sampling rate
- ii. multiplexing and demultiplexing
- iii. transmission of data by copper cable and fibre-optic cable

2 state the purpose of encoding data transmissions and recognise the forms

- i. RZ
- ii. Manchester
- iii. Gray code
- iv. Binary Coded Decimal

3 a identify employment of parity bits in a transmission system including

- i. advantages and disadvantages
- ii. odd and even parity using either data value of 0 or 1

b define the requirement for error detection and correction in digital transmission systems.

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Outcome 3 Demonstrate an understanding of sequential logic

Practical activities

The candidate will be able to:

1 assemble and test circuits using JK and D-type bistable integrated circuits

2 assemble and test shift registers using integrated circuits such as the 74XX194

3 assemble and test synchronous and asynchronous modulo-n counters using integrated circuits 74XX74, 74XX112, 74XX193 and 74XX390

4 use a counter to determine the degree of switch bounce occurring in a variety of toggle switches.

Underpinning knowledge

The candidate will be able to:

1 a define the circuit and waveforms associated with
   i. JK bistable
   ii. D-type bistable
   iii. Master-slave JK bistable

   b explain ways of connecting bistables to provide modulo-n dividers, and up/down counters

2 a describe synchronous and asynchronous integrated counters
   i. decade counters
   ii. modulo-n counters and dividers

   b define the associated timing diagrams and waveforms

3 a explain the circuit of a
   i. ring counter
   ii. twisted ring
   iii. shift register, using a universal shift register

   b determine the associated timing diagrams and waveforms

4 measure the degree of contact bounce for mechanically operated switches and relays.

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Outcome 4 Demonstrate an appreciation of common fault types and an understanding of faultfinding procedures and test equipment

Practical activities

The candidate will be able to:

1 use suitable test equipment to locate faults in digital interfacing circuits involving remote controls, A/D and D/A conversion and seven segment displays

2 use suitable test equipment to locate faults in synchronous and asynchronous counters, shift registers and bistable circuits

3 use suitable test equipment to locate faults in systems involving combinational logic circuits.

Underpinning knowledge

The candidate will be able to:

1 a determine the common causes of operational failure in integrated circuits due to

i. incorrect insertion into sockets

ii. shorting of pins during measurements

iii. poor soldering techniques

iv. insertion and removal with power supplies connected

v. incorrect voltages

vi. input pins left disconnected

vii. electrostatic discharge

b identify methods used to prevent damage due to electrostatic discharge

i. correct storage of ICs

ii. correct choice of floor coverings, clothing and worksurface

iii. correct use of wrist straps, heel straps and conductive matting

2 explain the use and limitations of the following items of test equipment

i. multimeter

ii. logic probe and logic clip

iii. logic pulser

iv. logic analyser

v. current tracer

vi. signature analyser

3 describe faultfinding techniques for

i. recording results of applied tests

ii. simple checks on plugs, connectors and power supplies

iii. one change at a time

iv. half-split method

v. input to output and output to input methods

Unit record sheet

Use this form to track your progress through this unit.

Tick the boxes when you have covered each outcome. When they are all ticked, you are ready to be assessed.

Outcome	✓	Date
1 Demonstrate an understanding of logic families and the terms used in their specifications	☐	
2 Demonstrate an understanding of time division multiplex (TDM)	☐	
3 Demonstrate an understanding of sequential logic	☐	
4 Demonstrate an appreciation of common fault types and an understanding of faultfinding procedures and test equipment	☐	
	☐	
	☐	

Candidate Signature ..... **Date** .....

City & Guilds Registration Number .....

Quality nominee (if sampled) ..... **Date** .....

Assessor Signature ..... **Date** .....

External Verifier Signature (if sampled) ..... **Date** .....

Centre Name ..... **Centre Number** .....

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